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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,109	BARRETT ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-19,21-27* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the Request for Reconsideration under 37 C.F.R. §1.111, and to the Remarks, filed 20 March 2006. Claims 1 – 27 are still pending in this Application.

Response to Remarks

2. Applicant's Remarks, filed 20 March 2006, with respect to the rejections of claims 1, 5 – 9, 12 – 19, 21, 22 and 24 - 27 under 35 U.S.C. 102(b) and claims 4, 10, 11 and 23 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejections are made in view of U.S. Patent No. 6,824,931 B2, and other prior art, as indicated below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 3, 5 – 7, 9, 12 – 19, 21, 22 and 24 – 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,824,931 B2 to Liu et al. (hereinafter, "Liu").

5. Pursuant to claim 1, Liu teaches a method for generating kerf (or scribe line) data (see Abstract; col. 4, ll. 31 – 37) that includes: (a) submitting chip data for chip processing (see col. 3, line 61 – col. 4, line 29); (b) generating kerf data corresponding to the chip data (see col. 6, ll. 10 – 25); and (c) manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data (see again col. 6, ll. 10 – 25, which cite SRAM/DRAM cells, requiring the same manipulation process as for the chip data). Thus, Liu discloses all the limitations as claimed.

6. Claims 21 and 27 contain the same limitations found in claim 1, and therefore the same rejections also apply.

7. As for claims 2 and 3, see again col. 6, ll. 10 – 67 which teach, or at the very least suggest, the claimed elements pertaining to just-in-time kerf circuit generation substantially immediately prior to mask manufacturing in order to avoid multiple versions of the kerf design.

8. Referring to claims 5 – 7, see (5) above; Fig. 7 and 8; col. 7, ll. 3 – 35 which teach the claimed limitations of sharing, accessing mask order information and using the same version of software to manipulate the chip design and kerf data.

9. Regarding claim 9, see col. 6,ll.10 – 37, which show the kerf test structures for wafer testing, as claimed.

10. As to claims 12 and 13, see also Figs. 5 and 6; col. 5, line 62 – col. 6, line 67, which disclose the claimed limitations pertaining to the generating/manipulating steps (claim 12) and the kerf/chip design images (claim 13).

11. Pursuant to claim 14, see (5) above and col. 4, ll. 38 – 63, which teach, or at the very least suggest, the elements pertaining to an audit process for debugging purposes, as claimed.

12. Regarding claim 15, Liu discloses a method for generating kerf data comprising: (a) executing design manipulation utilities for chip data design manipulation (col. 5, ll. 45 – 61); (b) creating a kerf design build utilities file by assembling kerf features previously designed and stored in a library of kerf design data as a result of kerf manipulation (see col. 6, ll. 10 – 67); and (c) creating and manipulating kerf design data concurrently with the chip data design manipulation processing by using same parameters in the kerf design data manipulation and chip data manipulation to ensure consistency (see col. 6, ll. 19 – 21, which shows representative memory cells in the kerf, thus ensuring consistency with the chip data). Liu thus recites all the claimed elements.

13. As per claims 16 and 17, see again col. 6, ll. 10 – 67, which teach the claimed limitations pertaining to shrinks, expands and new data levels in the design data (claim 16), and adding nonfunctional shapes as assist features to enhance processing latitude (claim 17).

14. Pursuant to claim 18, see (5) above and Fig. 7, block 706; col. 6, ll. 38 – 67; col. 7, ll. 3 - 16, which teach, or at the very least suggest, the claimed elements pertaining to archiving the modified design data in a design repository (since the patterns can also be standardized).

15. As to claim 19, see col. 6, ll. 13 – 25, which teach how pre-designed circuits (e.g., representative memory cells previously created and stored in a file) can be used in the kerf design, as claimed.

16. Claim 22 contains the same limitations as in claims 2 and 3, and thus the same rejections apply.

17. Claims 25 and 26 contain the same limitations as in claims 13 and 9, respectively, and therefore the same rejections apply.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 4, 10, 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Chiang et al. ("From CIF to Chips", 1989 IEEE Eighth Biennial University/ Government/Industry Symposium Proceedings).

20. As for claims 4, 10, 11 and 23, Liu teaches the method for generating kerf data by submitting chip data for processing and manipulating the kerf data, as recited above.

But Liu does not specifically disclose the claimed elements of using a graphical user interface (GUI), or communicating by email in order to facilitate debugging and reduce mean time to repair to reduce cycle time for the kerf processing, as claimed.

Chiang et al., on the other hand, discloses a VLSI design platform that includes a GUI interface (see graphical layout editor described on page 156, section entitle "**Background")** and also includes means for communicating via email to send error messages to all parties on the mailing list in order to improve debugging and reduce cycle time (see page 158, Figure 3, and section entitled "**The Fabrication Interface Service"**).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Parker and Chiang et al. because using a GUI and email facilities (which are both very well known and commonly used in this and other arts) would enhance, streamline and facilitate the debugging and characterization process cited by Parker.

21. **Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Parker et al. (U.S. Patent No. 6,330,708 B1).**

22. Liu teaches the method for generating kerf data by submitting chip data for processing and manipulating the kerf data, as recited above.

Liu does not teach using load balancing in processing chip design and kerf data.

But Parker et al. cites a method for preparing command files for photomask production, whereas the photomask contains chip design as well as kerf data (see Parker et al, col. 3, ll. 21 – 33), which also includes load balancing (see col. 2, ll. 34 – 48).

Since load balancing will speed up the processing and throughput of the data included in the chip design and in the kerf test circuits, it would therefore be obvious to a

person of ordinary skill in the art at the time of the invention to combine the teachings of Liu and Parker et al. to obtain the same claimed invention.

Allowable Subject Matter

23. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter: prior art does not teach, or suggest, the claimed method of submitting the kerf design data to validation checks to ensure that the combination of kerf design grid and chip design grid prevents grid snapping at the mask write tool.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
30 March 2006

MYD

A. M. Thompson
Primary Examiner
Technology Center 2800